IN THE CLAIMS:

Kindly replace the claims of record with the following full set of claims:

1. (Currently amended) A method of determining a maximum optimum clock frequency at which a digital processing system can operate, the method comprising the steps of:

generating a clock signal at an initial frequency;

increasing said frequency in a step-wise manner and determining the operation of said system each of a selected number of frequencies, until a clock frequency is identified at which said processing system ~~processor~~ does not operate correctly; and

identifying a maximum clock frequency at which said system can operate correctly; characterized in that:

said maximum clock frequency comprises the frequency immediately previous to the one identified as being one at which said system does not operate correctly; and in that

a timing monitor is provided for determining whether or not said processing system can operate within system timing constraints at each frequency, thereby indicating whether or not said system operates correctly at the respective frequency, said timing monitor monitoring at least a level of input and output buffers to prevent said output buffers from being starved of data while said input buffers include data that is blocked from said processing system.

2. (Original) A method according to claim 1, including the step of storing the maximum frequency in a memory.

3. (Previously amended) Method of calibrating clock generation means in a digital processing system, comprising periodically performing the method of claim 1 while the system is running and applying the resultant maximum frequency to said clock generation means.

4. (Currently amended) Apparatus for determining a maximum optimum clock frequency at which a digital processing system can operate, the apparatus comprising:

means for generating a clock signal at an initial frequency;

means for increasing said frequency in a step-wise manner and means for determining the operation of said system each of a selected number of frequencies, until a clock frequency is identified at which said processor does not operate correctly; and

means for identifying a maximum clock frequency at which said system can operate correctly; characterized in that:

said maximum clock frequency comprises the frequency immediately previous to the one identified as being one at which said system does not operate correctly; and in that

said means for determining the operation of said system comprises a timing monitor for determining whether or not said system can operate within system timing constraints at each frequency, thereby indicating whether or not said system operates correctly at the respective frequency, by monitoring at least a level of input and

output buffers to prevent said output buffers from being starved of data while said input buffers include data that is blocked from said processing system.

5. (Currently amended) A method of selectively changing the frequency at which a digital processing system is operating, the method comprising:

a) determining, when said system is reset, a maximum clock frequency at which said system can operate within system timing constraints, determining by maintaining a level of input and output buffers to prevent said output buffers from being starved of data while said input buffers include data that is blocked from said processing system, and storing said maximum frequency;

b) generating after reset, a clock signal at a nominal frequency, less than said maximum frequency, until a signal is received indicating that an increased clock frequency is required;

c) generating, in response to receipt of said signal, a clock signal at said maximum frequency for a required time; and then

d) once again generating a clock frequency at said nominal frequency.

6. (Currently amended) A method according to claim 5, wherein the step of determining said maximum frequency comprises:

generating a clock signal at an initial frequency;

increasing said frequency in a step-wise manner and determining the operation of said system each of a selected number of frequencies, until a clock frequency is identified at which said processing system ~~processor~~ does not operate correctly; and

identifying a maximum clock frequency at which said system can operate correctly; characterized in that:

said maximum clock frequency comprises the frequency immediately previous to the one identified as being one at which said system does not operate correctly; and in that

a timing monitor is provided for determining whether or not said system can operate within system timing constraints at each frequency, thereby indicating whether or not said system operates correctly at the respective frequency, said timing monitor monitoring at least a level of input and output buffers to prevent said output buffers from being starved of data while said input buffers include data that is blocked from said processing system.

~~the method of claim 1~~.

7. (Currently amended) Apparatus for selectively changing the frequency at which a digital processing system is operating, the apparatus comprising:

i. programmable clock generation means;

ii. means for determining when said system is reset, a maximum clock frequency at which said system can operate within system timing constraints determined by maintaining a level of input and output buffers to prevent said output buffers from being starved of data while said input buffers include data that is blocked from said processing system, and storing said maximum frequency; and

iii. means for causing said clock generation means to:

a) generate, after reset, a clock signal at a nominal frequency, less than said maximum frequency, until a signal is received indicating that an increased clock frequency is required:

b) generate, in response to receipt of said signal, a clock signal at said maximum frequency for a required time; and then

c) once again generate clock frequency at said nominal frequency.

8. (Previously amended) Apparatus according to claim 7, comprising a timing monitor for monitoring system timing constraints.

9. (Previously amended) Apparatus according to claim 4 comprising a frequency finder for increasing the frequency of the claim signal from the initial frequency to the maximum frequency.

10. (Previously amended) Apparatus according to claim 4, wherein said clock generation means comprises a programmable ring oscillator.

11. (Previously amended) Apparatus according to claims 7, comprising a frequency finder and selector for determining the maximum frequency at reset, receiving a request for an increase in clock frequency and causing the clock generation means to generated a clock signal at the maximum frequency until the request expires or is withdrawn.

12. (Currently amended) Apparatus according to claim 7, comprising:

a frequency finder for determining said maximum frequency at reset and causing said clock generation means to generate a clock signal at said maximum frequency,

said clock generation means comprising:

a first clock generation means and a second clock generation means, said second generation means arranged and configured to generate a clock signal at said nominal frequency, the outputs of the first and second clock generation means being coupled to a clock output by switch means, said switch means being arranged to couple the output of said second clock generation means to said clock output until a request to increase said clock frequency is received, in response to which, said switch means causes the output of said first clock generation means to be coupled to said clock output, until said request expires or is withdrawn.

13. (Previously amended) Apparatus according to claim 12, comprising means for disabling the first clock generation means when the request expires or is withdrawn.

14. (Previously amended) Apparatus according to claim 12, wherein the second clock generation means comprises an external clock generation means.